IN THE SPECIFICATION:

On page 12, lines 11-18, please amend the paragraph to read as follows:

Although the preferred embodiments have shown limited components the invention can have any number of registers, ALUs, internal memory and external memory of any size. Any component (ALU, register internal or external memory) can be connected together in many combinations and more than one connection can take place in one clock cycle. In the preferred embodiment the registers 14-28 are shown on the Y bus but they can be on the X bus or in any combinations on either bus. The buses can either be serial or parallel. Parallel bus will be quicker but to create a serial bus ie B=1 would be much easier as only one switch would be required per ~~bus~~ node unlike N switches for an N-bit bus.

B1
